3A Ultra Low Dropout Linear Regulator

General Description

The uP0132Q is a 3A ultra low dropout linear regulator specifically designed for motherboard and notebook applications. This device works with dual supplies, a control input for the control circuitry and a power input as low as 1.2V for providing current to output. The uP0132Q delivers high-current and ultra-low-drop output voltage as low as 0.8V for applications where V_{OUT} is very close to $V_{IN.}$

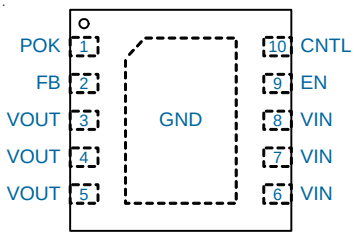
The uP0132Q features comprehensive control and protection functions: a power on reset (POR) circuit for monitoring both control and power inputs for proper operation; an EN input for enabling or disabling the device, a power OK with time delay for indicating the output voltage status, a current limit function, and a thermal shutdown function. The uP0132Q is available in WDFN3x3-10L package with very low thermal resistance.

Ordering Information

Order Number	Package Type	Top Marking
uP0132QDDA	WDFN3x3-10L	uP0132Q

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



WDFN3x3-10L

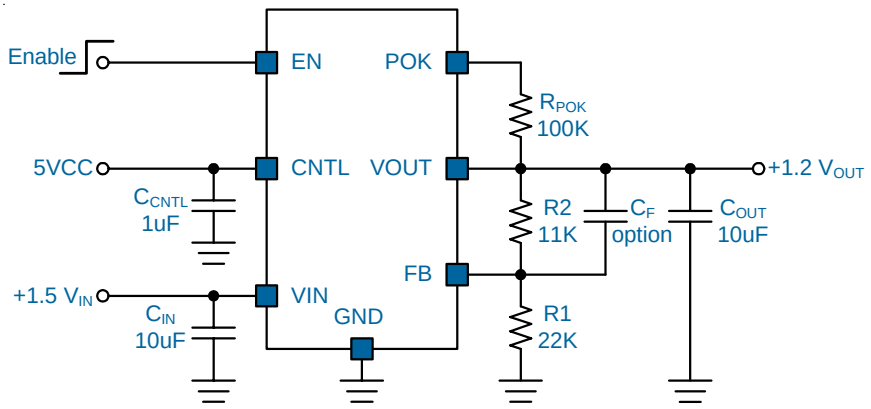
Features

- Works with 1.2V~5.5V V_{IN}
  - Adjustable Output Voltage, Down to 0.8V
  - 1.5% Initial Accuracy
  - Excellent Line and Load Regulation
- 3A Guaranteed Output Current
  - 120mV @ 2A Dropout Voltage
- Very Low On-Resistance
  - 60mΩ typical
- V_{OUT} Pull Low Resistance when Disabled
- Low Reverse Leakage (Output to Input)
- V_{OUT} Power OK Signal
- Fast Transient Response
- Low External Component Count
- Low Cost and Easy to Use
- Enable Pin (Internal Pull Low)
- Over Current and Over Temperature Protection
- RoHS Compliant and Halogen Free

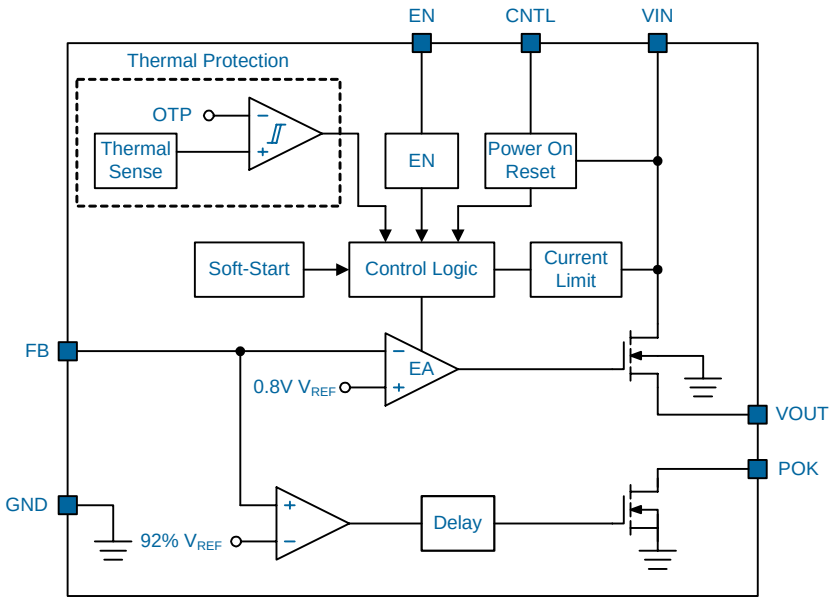
Applications

- Desktop PCs, Notebooks, and Workstations
- Graphic Cards
- Low Voltage Logic Supplies
- Microprocessor and Chipset Supplies
- Split Plane Microprocessor Supplies
- Advanced Graphics Cards Supplies
- SoundCards and Auxiliary Power Supplies
- SMPS Post Regulators

Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Pin No.	Name	Pin Function
1	POK	**Power OK Indication.** This pin is an open-drain output and is set high impedance once V_{OUT} reaches 92% of its rating voltage.
2	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage as V_{OUT} = 0.8(1+R2/R1) (V)
3, 4, 5	VOUT	**Output Voltage.** This pin is power output of the device. A pull low resistance exists when the device is disabled by pulling low the EN pin.
6, 7, 8	VIN	**Input Voltage.** This is the drain input to the power device that supplies current to the output pin. Using a ceramic capacitor which value is at least 10uF on the uP0132Q output for stability and improving transient response.
9	EN	**Enable Input.** Pulling this pin below 0.7V turns the regulator off, reducing the quiescent current to a fraction of its operating value. If this pin is floating, the regulator will enter shutdown mode.
10	CNTL	**Supply Input for Control Circuit.** This pin provides bias voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the VCNTL. For the device to regulate, the voltage on this pin must be at least 1.5V greater than the output voltage, and no less than V_{CNTL_MIN}.
Exposed Pad		**Ground.** The exposed pad acts the dominant power dissipation path and should be soldered to well design PCB pads as described in the Application Information Chapter.

Functional Description

Definitions

Some important terminologies for LDO are specified below.

Dropout Voltage

The input/ output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. When the output is drops 2% below its nominal value, the Dropout voltage is the voltage between the input and output voltage. Dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation

The change in output voltage for a change in load current at constant chip temperature. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Maximum Power Dissipation

The maximum total device dissipation for the regulator will operate within specifications.

Initialization and POR

The uP0132Q automatically initiates upon the receipt of supply voltage and power voltage. A power on reset circuit continuously monitors V_{IN} and V_{CNTL} pins voltages with rising threshold levels of 0.8V and 2.7V respectively.

Chip Enable

The uP0132Q features an enable pin for enable/disable control of the chip. Pulling VEN lower than 0.7V disables the chip and reduces its quiescent current down to 1uA. When disabled, an internal MOSFET of 90Ω $R_{DS(ON)}$ turns on to pull output voltage to ground. Pulling VEN higher than 1.4V enables the output voltage, providing POR is recognized. If EN pin is floating, the regulator will enter shutdown mode.

Soft Start

The uP0132Q features soft start function that limits inrush current for charging the output capacitors. The soft start time is typically 2ms.

Voltage Programming

Figure 1 shows a typical application of 1.5V to 1.2V conversion with a 5.0V control supply. The output voltage is sensed through a voltage divider and regulated to internal reference voltage V_{REF}. The output voltage is programmed as:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right) = 0.8V \times \left(1 + \frac{11K}{22K}\right) = 1.2V$$

The internal voltage reference is V_{REF} = 0.8V with 1.5% accuracy over full temperature range. This commands the use of 0.5% or better accuracy resistors to build a precision power supply.

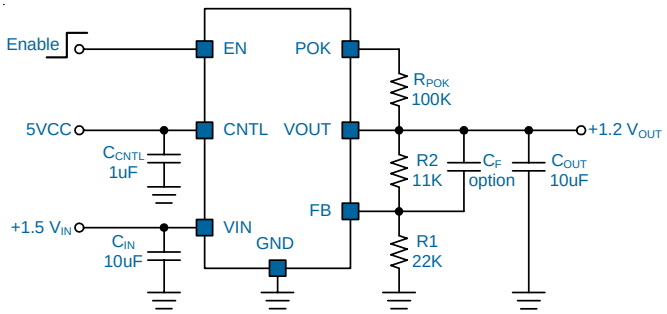


Figure1. Typical application of 1.5V to 1.2V conversion with a 5.0V control supply.

Power OK Indication and Delay

The POK pin is an open drain output that is asserted high impedance with time delay after the soft-start cycle is competes as long as the output voltage is within its regulation band. The uP0132Q features POK function for indicates the status of the output voltage by detecting FB pin voltage, V_{FB}. When the rising V_{FB} greater then setting POK threshold and after a period of delay time. At the end of the delay time, the IC pulls high the POK voltage to indicate the output is OK. As the FB voltage falls and reaches the falling Power-OK hysteresis, the IC pull down the POK voltage to indicate the output is not OK without a delay time.

Current-Limit Protection

The uP0132Q monitors the current via the output NMOS and limits the maximum current to 3.6A typical to prevent load and uP0132Q from damages during over current conditions.

Short Current-Limit Protection

In the end of soft-start, the uP0132Q will enable short current-limit function which maintains the loading current at maximum 1.8A when V_{OUT} is less than 0.2V.

Over Temperature Protection

The over temperature protection limits total power dissipation in the uP0132Q when the junction temperature exceeds T_J = 150°C, the thermal sensor signal the shutdowns logic, turning off the pass transistor and allows the device to cool down. The thermal sensor turns on the pass transistor again after the devices junction temperature drops by 30°C, resulting in a pulsed output during continuous thermal-overload conditions. The over temperature protection is designed to protect the device in the event of a fault condition. For continual operation, do not exceed the recommended temperature of T_J = 125°C for maximum reliability. The over current protection and thermal shutdown protection behavior is shown in figure 2 below.

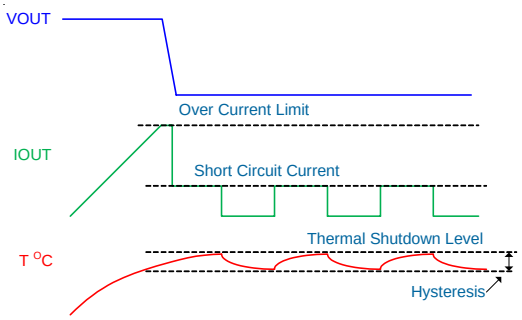


Figure 2. Over Current Protection and Thermal Shutdown Protection

Absolute Maximum Rating

(Note 1)

Control Input Voltage V_{CNTL}
- DC ---------- -0.3V to +6.5V
- < 200ns ---------- -0.3V to +7.0V

Power Input Voltage V_{IN}
- DC ---------- -0.3V to +6.5V
- < 200ns ---------- -0.3V to +7.0V

Other Pins ---------- -0.3V to (V_{CNTL} + 0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3/4)
- WDFN3x3 - 10L θ_{JA} ---------- 68°C/W
- WDFN3x3 - 10L θ_{JC} ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C
- WDFN3x3 - 10L ---------- 1.47W

Recommended Operation Conditions

(Note 5)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Control Input Voltage, V_{CNTL} ---------- 3V to 5V
Supply Input Voltage, V_{IN} ---------- 1V to 5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-5 thermal measurement standard.

Note 4. The “case temp” location for measuring q_{JC} is on the top of the package.

Note 5. The device is not guaranteed to function outside its operating conditions.

Note 6. This test item is tested under constant junction temperature which does not exceed absolute maximum ratings. In this test, a 5ms current pulse is applied at the output for measuring required data without exceeding junction temperature AMR.

Note 7. This test item is tested under constant junction temperature which does not exceed absolute maximum ratings. In this test, the dropout voltage is measured as V_{IN}-V_{OUT} where V_{IN} equals $V_{OUT,NOMINAL}$-100mV, and V_{OUT} decreases lower than $V_{OUT,NOMINAL}$ due to IR drop.

Note 8. OCP threshold level is not guaranteed to function outside its linear region.

Electrical Characteristics

(V_{CNTL} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
Control Input Voltage	V_{CNTL}	V_{OUT} = V_{REF}	3.0	--	5.5	V
POR Threshold	$V_{CNTLRTH}$	V_{CNTL} rising	2.5	2.7	2.9	V
POR Hysteresis	$V_{CNTLHYS}$	V_{CNTL} falling	--	0.2	--	V
Power Input Voltage	V_{IN}	V_{OUT} = V_{REF}	1	--	5.5	V
VIN POR Threshold	V_{INTH}	V_{IN} rising	--	0.8	--	V
VIN POR Hysteresis	V_{INHYS}	V_{IN} falling	--	0.4	--	V
Control Input Current in Shutdown	I_{CNTL_SD}	V_{CNTL} = V_{IN} = 5.0V, I_{OUT} = 0A, V_{EN} = 0V	--	--	1	uA
Control Input Current	I_{CNTL}	V_{CNTL} = V_{IN} = V_{EN} = 5.0V, I_{OUT} = 0A, V_{OUT} = V_{REF}	--	0.25	--	mA
Quiescent Current	I_Q	V_{CNTL} = V_{IN} = V_{EN} = 5.0V, I_{OUT} = 0A, V_{OUT} = V_{REF}	--	0.05	--	mA
Enable						
Enable High Level	V_{EN}		1.4	--	--	V
Disable Low Level	V_{SD}		--	--	0.7	V
EN Sink Current	I_{EN}	VEN = 5V	--	5	--	uA
Enable Delay Time	T_{DELAY}	From being enabled to V_{OUT} rising 10%	--	250	--	us
Output Ramp Up Time	T_{SS}	Form V_{OUT}=10% to 92% of $V_{OUT,NOM}$	--	2	--	ms
Feedback Voltage						
Reference Voltage	V_{REF}	V_{CNTL} = V_{IN} = V_{EN} = 5.0V, I_{OUT} = 0A, V_{OUT} = V_{REF}	0.792	0.800	0.808	V
Feedback Input Current	I_{FB}		--	20	--	nA
V_{IN} Line Regulation	$V_{REF(LINE)}$	1.2V < V_{IN} < 5.0V, V_{CNTL} = V_{EN} = 5.0V, I_{OUT} = 0A	--	0.01	0.1	%/V
V_{CNTL} Line Regulation	$V_{REF(CNTL)}$	3V < VCNTL < 5.0V, V_{IN} = 1.2V, I_{OUT} = 0A, V_{OUT} = V_{REF}	--	0.01	0.1	%/V
Load Regulation (Note6)	$V_{REF(LOAD)}$	10mA < I_{OUT} < 3A, V_{CNTL} = V_{EN} = 5.0V, V_{IN} = V_{OUT}+0.5V	--	0.8	1.5	%/A
Dropout Voltage (Note7)	V_{DROP}	I_{OUT} = 2A, V_{CNTL} = V_{EN} = 5.0V, V_{IN} = $V_{OUT,NOMINAL}$-100mV	--	120	180	mV
		I_{OUT} = 3A, V_{CNTL} = V_{EN} = 5.0V, V_{IN} = $V_{OUT,NOMINAL}$-100mV	--	180	270	
V_{OUT} Pull Low Resistance		V_{CNTL} = V_{IN}, V_{EN} = 0V,	--	90	150	Ω

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
PWROK						
Power OK Threshold	V_{POKTH}	V_{FB} rising	--	92	--	$\%V_{FB}$
Power OK Hysteresis	V_{POKHYS}	V_{FB} falling	--	8	--	$\%V_{FB}$
POK Delay Time	T_{DELAY}	From V_{OUT} > 92% $V_{OUT,NOM}$ to POK rising	--	300	--	us
Over Current Protection						
Current Limit Threshold (Note8)	I_{LIM}	V_{CNTL} = 3.3V	3.1	3.6	4.1	A
Short Circuit Current	V_{SHORT}	V_{OUT} < 0.2V	1	1.5	1.8	A
Over Temperature Protection						
Thermal Shutdown Temperature	T_{SD}	V_{CNTL} = V_{IN} = V_{EN} = 5.0V, I_{OUT} = 0A, V_{OUT} = V_{REF}	--	150	--	^{O}C
Thermal Shutdown Hysteresis	T_{SDHYS}	V_{CNTL} = V_{IN} = V_{EN} = 5.0V, I_{OUT} = 0A, V_{OUT} = V_{REF}	--	30	--	^{O}C

Application Information

The uP0132Q is a high performance linear regulator specifically designed to deliver up to 3A output current with very low input voltage and ultra low dropout voltage. With dual-supply configuration, the uP0132Q operates with a wide input voltage V_{IN} range from 1.0V to 5.5V and is ideal for applications where V_{OUT} is very close to V_{IN}.

Supply Voltage for Control Circuit V_{CNTL}

Unlike other linear regulators that use a P-Channel MOSFET as the pass transistor, the uP0132Q uses an N-Channel as the pass transistor. N-Channel MOSFET provides lower on-resistance and better stability meeting stringent requirements of current generation microprocessors and other sensitive electronic devices. The drain of N-Channel MOSFET is connected to V_{IN} and the source is connected to V_{OUT}. This requires that the supply voltage VCNTL for control circuit is at least 1.5V higher than the output voltage to provide enough overdrive capability for the pass transistor thus to achieve low dropout and fast transient response. It is highly recommended to bias the device with 5V voltage source if available. Use a minimum 0.1uF ceramic capacitor plus a 10Ω resistor to locally bypass the control voltage.

Input Capacitor

A minimum of 10uF ceramic capacitor is recommended to be placed directly next to the V_{IN} pin. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, bulk capacitance may be added closely to the input supply pin of the uP0132Q to ensure that V_{IN} does not sag, improving load transient response.

Output Capacitor

Please be certain the output capacitors are connected between V_{OUT} pin and GND to assure output voltage stability. A minimum of 10uF ceramic capacitor is recommended, actual stability is highly dependent on temperature and load conditions. Increasing the bulk capacitance will improve the overall transient response. The use of multiple lower value ceramic capacitors in parallel to achieve the desired bulk capacitance will not cause stability issues. Although designed for use with ceramic output capacitors, the uP0132Q is extremely tolerant of output capacitor ESR values and thus will also work comfortably with tantalum output capacitors.

Thermal Consideration

The uP0132Q integrates internal thermal limiting function to protect the device from damage during fault conditions. However, continuously keeping the junction near the thermal shutdown temperature may remain possibility to affect device reliability. It is highly recommended to keep the junction temperature below the recommended operation condition 125°C for maximum reliability.

Power dissipation in the device is calculated as:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{CNTL} \times I_{CNTL}$$

It is adequate to neglect power loss with respective to control circuit V_{CNTL} x I_{CNTL} when considering thermal management in uP0132Q. Take the following moderate operation condition as an example: V_{IN} = 3.3V, V_{OUT} = 2.5V, I_{OUT} = 1.8A, the power dissipation is:

$$P_D = (3.3V - 2.5V) \times 1.8A = 1.44W$$

This power dissipation is conducted through the package into the ambient environment, and, in the process, the temperature of the die (T_J) rises above ambient. Large power dissipation may cause considerable temperature raise in the regulator in large dropout applications. The geometry of the package and of the printed circuit board (PCB) greatly influence how quickly the heat is transferred to the PCB and away from the chip. The most commonly used thermal metrics for IC packages are thermal resistance from the chip junction to the ambient air surrounding the package (θ_{JA}):

$$\theta_{JA} = \frac{(T_J - T_A)}{P_D}$$

θ_{JA} specified in the Thermal Information section is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the exposed pad for WDFN3x3 - 10L package.

Given power dissipation P_D, ambient temperature and thermal resistance θ_{JA}, the junction temperature is calculated as:

$$T_J = T_A + \Delta T_J = T_A + P_D \times \theta_{JA}$$

To limit the junction temperature within its maximum rating, the allowable maximum power dissipation is calculated as:

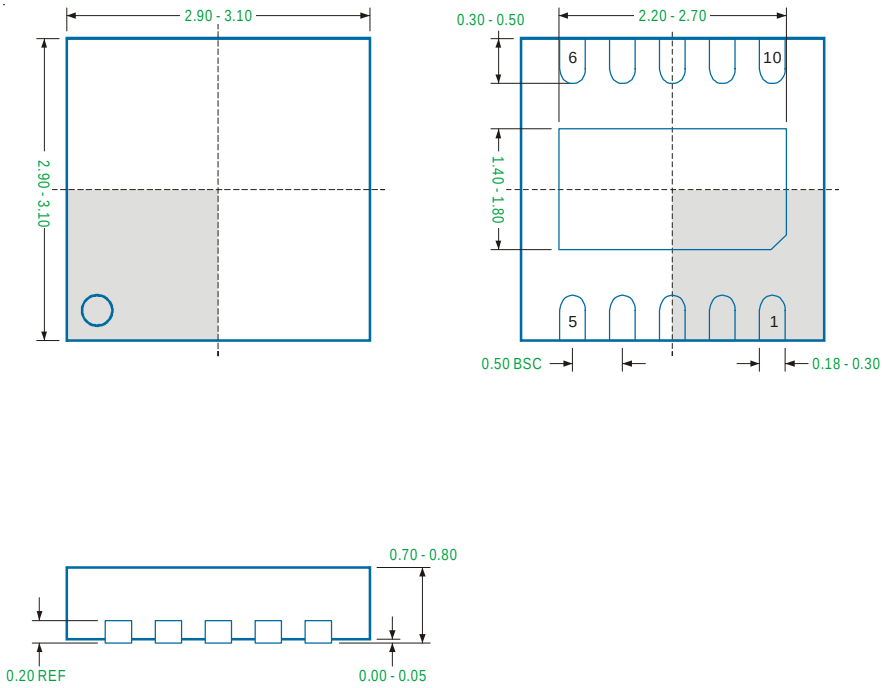
$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, TA is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. θ_{JA} of WDFN3x3 - 10L packages is 68°C/W on JEDEC 51-7 (4 layers, 2S2P) thermal test board with minimum copper area. The maximum power dissipation at T_A = 25°C can be calculated as:

$$P_{D(MAX)} = \frac{(125°C - 25°C)}{68°C/W} = 1.47W$$

Package Information

WDFN3x3-10L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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